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EXAMINER	
NGUYEN, JOSEPH H	
ART UNIT	PAPER NUMBER
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/554,541	HIRANO, HIROSHIGE	
	Examiner	Art Unit	
	JOSEPH NGUYEN	2815	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *13 January 2009*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-10* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-10* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *25 July 2008* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1-4 and 8-10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lee (U.S. Publication No. 2001/0025976) in view of Takenaka (U.S. 6,339,008) and further in view of Nam (U.S. Publication No. 2003/0057464).

Regarding claim 1, Lee discloses in figure 5 a ferroelectric memory device comprising a plurality of memory cell capacitors, each respective memory cell capacitor comprises a lower electrode 53 connected to a bit line; a ferroelectric layer 55 formed on an upper surface of the lower electrode and having a width direction that is the same as a width direction of the lower electrode; and an upper electrode 57 formed on an upper surface of the ferroelectric layer and having a width direction that is the same as the width direction of the lower electrode, wherein the lower electrodes 53 are independent from one another, wherein the upper electrodes 57 form a continuous plate electrode covering the lower electrodes. Lee does not disclose the width of said respective upper electrode is narrower than the width of the respective ferroelectric layer. However, Takenaka discloses in figure 1(e) a ferroelectric memory device comprising the width of the respective upper electrode 9 is narrower than the width of

the respective ferroelectric layer 8. In view of such teaching, it would have been obvious at the time of the present invention to modify Lee by including the width of said respective upper electrode being narrower than the width of the respective ferroelectric layer so as to so as to efficiently form the upper electrode and the lower electrode in an effective manner for certain application or design purpose.

Further, Lee and Takenaka do not disclose the ferroelectric memory device comprising a plurality of memory cell transistors. However, Nam discloses in figure 4 the ferroelectric memory device comprising a plurality of memory cell transistors 204 so as to fully form a ferroelectric cell memory device. In view of such teaching, it would have been obvious at the time of the present invention to modify Lee and Takenaka by including the ferroelectric memory device comprising a plurality of memory cell transistors so as to fully form a ferroelectric cell memory device.

Regarding claim 2, Nam discloses in figure 4 the width of each respective lower electrode 216 is narrower than the width of each respective ferroelectric layer 218.

Regarding claims 3-4, Takenaka discloses in column 6, lines 25-31 the upper electrode 9 and the lower electrode 4 are of the same size. In other words, Takenaka discloses the width of the upper electrode and the width of the lower electrode being substantially the same.

Regarding claim 8, Lee discloses in figure 5 each respective lower electrode 53 includes a groove type structure.

Regarding claim 9, Lee discloses in figure 5 a grooves formed in each respective lower electrode 53 extends along a direction that is parallel to a direction along which each respective upper electrode 57 extends.

Regarding claim 10, Lee discloses in figure 5 a direction along which a groove formed in each respective lower electrode 53 extends is perpendicular to a direction along which each respective upper electrode extends.

3. Claim 5 is rejected under 35 U.S.C. 103(a) as being unpatentable over Lee and Nam and further in view of Yamada et al. (U.S. Publication No. 2002/0096771).

Regarding claim 5, similar to rejection of claim 1 above, Lee and Nam together disclose substantially all the structure set forth in claim 5 except for a position of one edge of each respective upper electrode substantially aligning with a position of one edge of each respective ferroelectric and another edge of each respective upper electrode being inwardly located at a position relative to another edge of each respective ferroelectric layer. However, Yamada et al. discloses in figure 1 a capacitor comprising a position of one edge of each respective upper electrode 11 substantially aligning with a position of one edge of each respective ferroelectric 10 and another edge of each respective upper electrode 11 being inwardly located at a position relative to another edge of each respective ferroelectric layer 10. In view of such teaching, it would have been obvious at the time of the present invention to further modify Lee and Nam by including a position of one edge of each respective upper electrode substantially aligning with a position of one edge of each respective ferroelectric and

another edge of each respective upper electrode being inwardly located at a position relative to another edge of each respective ferroelectric layer so as to selectively form a capacitor in a desired manufacturing method for certain application or design purpose.

4. Claims 6-7 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lee and Nam and further in view of Yamada et al. and further in view of Ohno (U.S. Patent No. 5,923,062).

Regarding claim 6, Lee and Nam and further in view of Yamada et al. together disclose substantially all the structures set forth in claim 6 except for one edge of each respective lower electrode being inwardly located at a position relative to one edge of each respective upper electrode and a position of another edge of each respective lower electrode substantially aligning with a position of another edge of each respective upper electrode. However, Ohno discloses in figure 4G a memory cell device comprising one edge of each respective lower electrode 313a being inwardly located at a position relative to one edge of each respective upper electrode 316 and a position of another edge of each respective lower electrode313a substantially aligning with a position of another edge of each respective upper electrode 316 so as to suppress the leakage current of a capacitor (column 3, lines 3-4). In view of such teaching, it would have been obvious at the time of the present invention to further modify Lee and Nam and further in view of Yamada et al. by including one edge of each respective lower electrode being inwardly located at a position relative to one edge of each respective upper electrode and a position of another edge of each respective lower electrode

substantially aligning with a position of another edge of each respective upper electrode so as to suppress the leakage current of a capacitor.

Regarding claim 7, Lee and Nam and further in view of Yamada et al. together disclose substantially all the structures set forth in claim 7 except for one edge of each respective lower electrode being inwardly located at a position relative to one edge of each respective ferroelectric layer and a position of another edge of each respective lower electrode substantially aligning with a position of another edge of each respective ferroelectric layer. However, Ohno discloses in figure 4G one edge of each respective lower electrode 313a being inwardly located at a position relative to one edge of each respective ferroelectric layer 315 and a position of another edge of each respective lower electrode 313a substantially aligning with a position of another edge of each respective ferroelectric layer 315 so as to suppress the leakage current of a capacitor (column 3, lines 3-4). In view of such teaching, it would have been obvious at the time of the present invention to further modify Lee and Nam and further in view of Yamada et al. by including one edge of each respective lower electrode being inwardly located at a position relative to one edge of each respective ferroelectric layer and a position of another edge of each respective lower electrode substantially aligning with a position of another edge of each respective ferroelectric layer so as to suppress the leakage current of a capacitor (column 3, lines 3-4).

Response to Arguments

5. Applicant's arguments with respect to claims 1-10 have been considered but are moot in view of the new ground(s) of rejection.

6. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Conclusion

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Joseph Nguyen whose telephone number is (571) 272-1734. The examiner can normally be reached on Monday-Friday, 8:30 am- 5:00 pm. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Ken Parker can be reached on (571) 272-2298. The fax phone number for

the organization where this application or proceeding is assigned is (571) 273-8300 for regular communications.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

/J. N./

Examiner, Art Unit 2815

/Kenneth A Parker/

Supervisory Patent Examiner, Art Unit 2815